Broadband Time-Domain Characterization of Multiple Flip-Chip Interconnects

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Abstract **This paper presents a comprehensive approach for the characterization of multiple flip-chip interconnects by three-dimensional finite-difference time-domain (FDTD) method. The behaviors of transition discontinuities in three coplanar waveguide (CPW) layers and four flip-chip bump interconnects are investigated for optimal packaging performance. The relationship between the reflection loss and the cross-section of bumps is discussed in detail. Results in this paper shows that FDTD is a reliable method to simulate and aid design of complicated package structures.**

I. INTRODUCTION

Flip-chip interconnect is a popular surface mount packaging technique because it does not have lateral leads or pins and has advantages, such as low electrical parasitic and low-cost, easy assembly through self-alignment, the smallest footprint, and the thinnest profile and weight [1,2].

One important topic for flip-chip package is how to enhance the transition performance at operating frequency range. There are many parameters which affect the performance, such as the interconnect bump length and width, the conductor on the board below the chip, the feeding line width of CPW, and the ground to ground distance of CPW. Various methods have been applied to tune these parameters for optimal packaging performance [1,3,4,5], but they were limited to few structural variations. Solution of electromagnetic (EM) field is required for most of the packaging analyses, preferably broadband technique for high-speed circuitry. Flip-chip interconnect was studied by Sonnet simulation in comparison with experiment measurements [1], the simulation result was quite different from measured results, probably because incomplete modeling of the contributing factors to the transition performance, such as via pad size, via cross section and height, and dielectric layer. Two flip-chip with one interconnect was analyzed recently [3,4], they also gave broadband solutions. However, structure with three CPW layers connected by two sets of interconnect (via and ball), which is more complicated and close to actual design, has not been studied in detail.

FDTD method is a widely used full-wave time-domain simulation method used in the design and analysis for EM systems, such as antennas, wave propagating, and microwave circuits [6]. Absorbing boundary condition like perfect matched layer (PML) method [7] makes it possible to accurately analyze an EM structure involving complicated wave propagation in three-dimensional domain. Instead of running simulation at each frequency point like a frequency-domain EM method, time-domain solution gives complete frequency-domain response that includes coupling and dispersion effects.

This paper presents a wideband approach for characterizing multiple flip-chip interconnects by FDTD method. Detailed analysis for electrical performance for frequency up to 40 GHz has been performed with variations of interconnect bumps (ball cross section and via cross section). A three-layer CPW connected by two sets of interconnects (via and ball) is studied using FDTD method in detail. The relationship between reflection loss, ball cross-section and via cross section is tabulated for future packaging design. Based on the simulation results, some design approaches are proposed for packaging structure operating at near 40 GHz.

II. METHOD

Maxwell's equations, listed in (1), are the starting point for solving electromagnetic field distribution.

$$\oint_C \boldsymbol{E} \cdot d\boldsymbol{l} = -\int_S m \frac{\partial \boldsymbol{H}}{\partial t} \cdot d\boldsymbol{S} \tag{1a}$$

$$\oint_C \boldsymbol{H} \cdot d\boldsymbol{l} = \int_S (s\boldsymbol{E} + e\frac{\partial \boldsymbol{E}}{\partial t}) \cdot d\boldsymbol{S} \tag{1b}$$

Since the general three-dimensional finite-difference expressions are well known [6], for

reference purpose only the equations for z-components in Cartesian coordinate are listed here.

$$H_{zijk}^{n+1/2} = H_{zijk}^{n-1/2} + \frac{dt}{m}\left(\frac{E_{xij+1k}^{n} - E_{xijk}^{n}}{dy} + \frac{E_{yijk}^{n} - E_{yi+1jk}^{n}}{dx}\right) \quad (2a)$$

$$E_{zijk}^{n+1} = \frac{\frac{e_{ijk}}{dt} - \frac{s_{ijk}}{2}}{\frac{e_{ijk}}{dt} + \frac{s_{ijk}}{2}} E_{zijk}^{n} + \frac{1}{\frac{e_{ijk}}{dt} + \frac{s_{ijk}}{2}}\left(\frac{H_{yijk}^{n+1/2} - H_{yi-1jk}^{n+1/2}}{dx} + \frac{H_{xijk}^{n+1/2} - H_{xij-1k}^{n+1/2}}{dy}\right) \quad (2b)$$

Scattering (S) parameters of a given structure can be obtained by FDTD simulation. S parameters for a two port network is defined as:

$$\begin{bmatrix} v_r^1 \\ v_r^2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} v_i^1 \\ v_i^2 \end{bmatrix} \quad (3)$$

where superscripts 1 and 2 are port indices, and subscripts *r* and *i* refer to reflected and incident signals, respectively.

In order to obtain the S parameters at port 1, namely s_{11} and s_{12}, FDTD simulation should be run twice. First, the input signal s_i^1 is obtained for the distributed structure that has only the feeding CPW. Second, the total signal s_i^1 is calculated, it is the summation of the input and reflected signals with the effects of interconnects and other discontinuities in the system. Then the reflected signal can be calculated from the total signal and input signal. The reflection parameter can then be obtained by Fourier transform [8]

$$S_{11} = \frac{fft(v_t^1)}{fft(v_i^1)} \quad (4).$$

III. SIMULATION AND DISCUSSION

The multiple flip-chip interconnect structure used in this paper is based on thin film ceramic ball grid array (BGA) package [1,2]. The original structure has 3 RF and 5 DC I/O's. Figure 1 shows the side and top views of the simplified structure used for this study. There are three 50Ω CPWs and three associated dielectric layers. Layer substrates are alumina for the top and bottom layers, and air for the middle one, with heights of H1, H2 and H3, respectively. The dielectric constant for alumina is 9.6. Both input and output ports are on the bottom CPW line as shown in Figure 1(a). The metal layers are assumed perfect conductors (PEC) and of negligible thickness. There are two types of interconnect bumps: ball connecting CPW line 1 and line 2, and via connecting CPW line 2 and line 3. The round ball geometry is approximated as square and the RF via is also simplified as having a rectangular cross section.

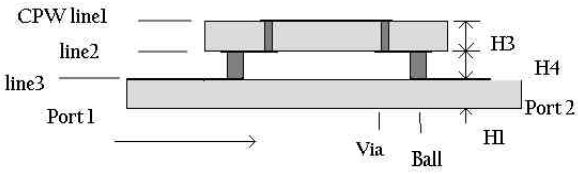

Figure 1(a). Side view of the three-layer structure. H1, H2, and H3 are 15 mils. The single arrow stands for the signal feeding direction.

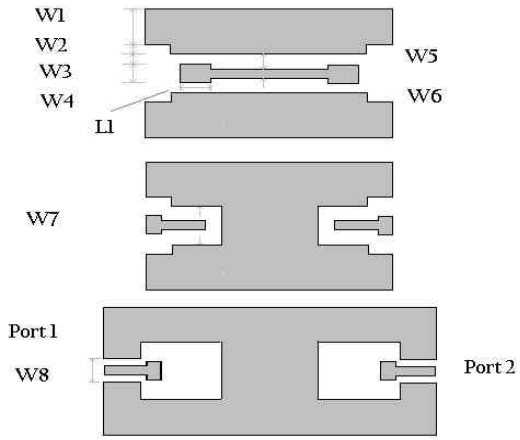

Figure 1(b). Top view of three CPW layers. W1, W2, W3 and W4 are 30, 10, 6, and 16 mils, respectively.

PML boundary condition in a non-uniform FDTD grid, 160x54x31 with average grid size of 50.8 mils, follows algorithm described in [9]. The workstation used for simulation is a Sun E5500 server; the average simulation time is 6-8 hours.

Figure 2 shows a comparison of reflection loss S11 between FDTD simulation and measurement and Sonnet simulation results reported in [1]. The closer match between FDTD result and measured data demonstrates the accuracy of the FDTD method. It proved that FDTD is an effective package simulation method; in the following FDTD is applied to optimize some interconnect bump packaging structures.

Ball and via interconnects can be described as an equivalent circuit of capacitance and inductance [5]. Changing ball cross section will change capacitance and inductance in the system, therefore causing reflection loss change at certain frequency range. FDTD simulation results demonstrated this behavior, as showing in Figure 3 where S11 is plotted versus different ball cross section when via cross section is set at 4x4 mil. The reflection coefficient becomes smaller as the ball cross-area increases from 4x4 to 16x16 mil. The reflection coefficient increases with

the increase of the cross section area when it is larger than 16x16 mil. This suggests that the package in this BGA format is useable in the frequency range of DC to 36 GHz if appropriate ball cross-section is chosen.

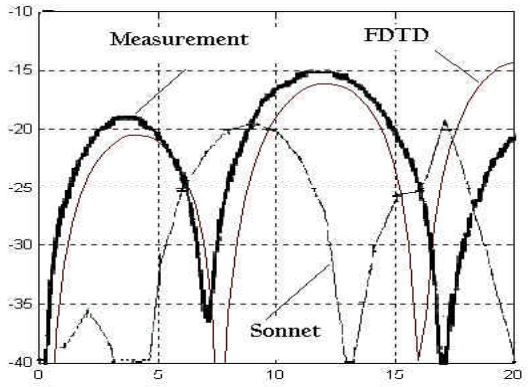

Figure 2. Comparison of S11, in dB vs. frequency in unit of GHz, from measurement and Sonnet simulation with FDTD result. W5, W6, W7, W8 and L1 are 4, 8, 24, 16 and 40 mils, respectively.

As shown in Figure 1(a), via bump connects CPW line 2 and line 3. In order to study its effects to the packaging performance, its cross section is changed in parallel and perpendicular to feeding direction. The effective inductance becomes larger when via size is increased along signal propagating direction. The larger inductance degrades signal transition for flip chip. This is in agreement with FDTD simulation result as shown in Figure 4 where S11 changes with via length along propagating direction. The structure with via size 8x4 mil has better transition at higher frequency near 30 GHz. However, the structure with 4x4 mil has overall better performance near lower frequency range.

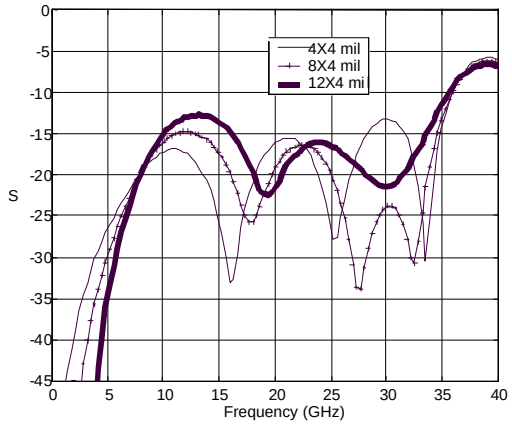

Figure 4. S11 for different via size along propagating direction. Via sizes are 4x4, 8x4 and 12x4 mil.

Tuning effective via capacitance can improve flip chip interconnect transition, the parameters which can contribute to via capacitance are via pad length [5] and via width perpendicular to feeding direction. Figure 5 shows that S11 changes with via width perpendicular to propagating direction. Structure with via size of 4x12 has the lowest reflection near 30 GHz, but 4x8 structure has the best performance from 0-40 GHz.

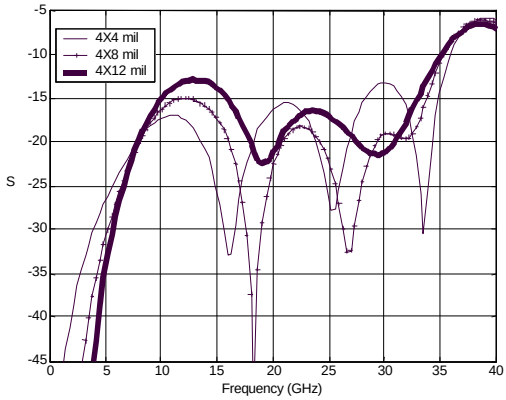

Figure 5. S11 for different via size perpendicular to propagating direction. Via sizes are 4x4, 4x8 and 4x12 mil.

It is reported that the cross-section area of bump or via does not affect S parameter significantly [10]. In their structure, there was only one via along the feeding line that connects two CPW lines and it was only half of structure studied here along the feeding direction. There are two sets of ball and via which vertically connect three CPW in this paper. Ball to ball, via to via and ball to via resonance affect s-parameter significantly. Simulation results presented here indicate that S11 parameter is sensitive to ball and via cross section and they illustrate several flip-chip structures can achieve a good transition design of 80% bandwidth over which the return loss is smaller than -20DB.

IV. Conclusions

FDTD simulation results show that via and ball effects can change the designed packaging structure performance significantly. S11 can be optimized for certain frequency by changing the size and shape of the ball and via. However, it is difficult to obtain a concise rule for choosing the optimized via or ball cross section at an arbitrary desired frequency band; FDTD method, nevertheless, provides an accurate and efficient approach to study the performance of the interested structure.

References

[1] PR Panicker et al., "Ball Grid Arrays: A DC to 31.5GHz Low Cost Packaging Solution for Microwave and MM-wave MMICs" *Microwave Journal*, Vol.41, No.1, January 1998, pp.

[2] *US Patent* No. 4,942,076, No. 5,832,598.

[3] H. M. Ghouz and E. EL-Aharawy, "Finite-difference time-domain analysis of flip-chip interconnects with staggered bumps" *IEEE Trans. Microwave Theory Tech*., vol.44, pp.963, June 1996

[4] H. M. Ghouz and E. EL-Aharawy, "An accurate equivalent circuit model of flip chip and via interconnects" *IEEE Trans. Microwave Theory Tech*., vol.44, pp.2550, Dec. 1996

[5] W. Heinrich, A. Jentzch, and G. Baumann, "Millimeterwave characteristics of flip-chip interconnects for multi-chip modules," *IEEE MTT-Symp. Dig.,* 1998, pp.1083-1086.

[6] A. Taflove, *Computational electrodynamics: The finite-difference time-domain method*, Artech House, Boston 1995.

[7] Berenger, J. P."A Perfectl matched Layer for The Absorption of electromagnetic Wave," *Journal of Computational Physics* 114, pp.185-200, 1993

[8] Tong Li, "FDTD-Based Full Wave Co-simulation Model for Hybrid Electromagnetic Systems," Ph.D. dissertation, New Jersey Institute of Technology, Newark, May 1999.

[9] T. Li, W. Sui and M. Zhou, "Extending PML absorbing boundary condition to truncate microstrip line in nonuniform 3D FDTD grid," *IEEE Transaction on MTT*, No. 9, Vol. 47, pp. 1771-1776, 1999.

[10] J. Kim, D. Koh, T. Itoh, "A Novel Broadband Flip Chip Interconnection" *Proc. IEEE MTT-S Digest*, p199-202, 1997

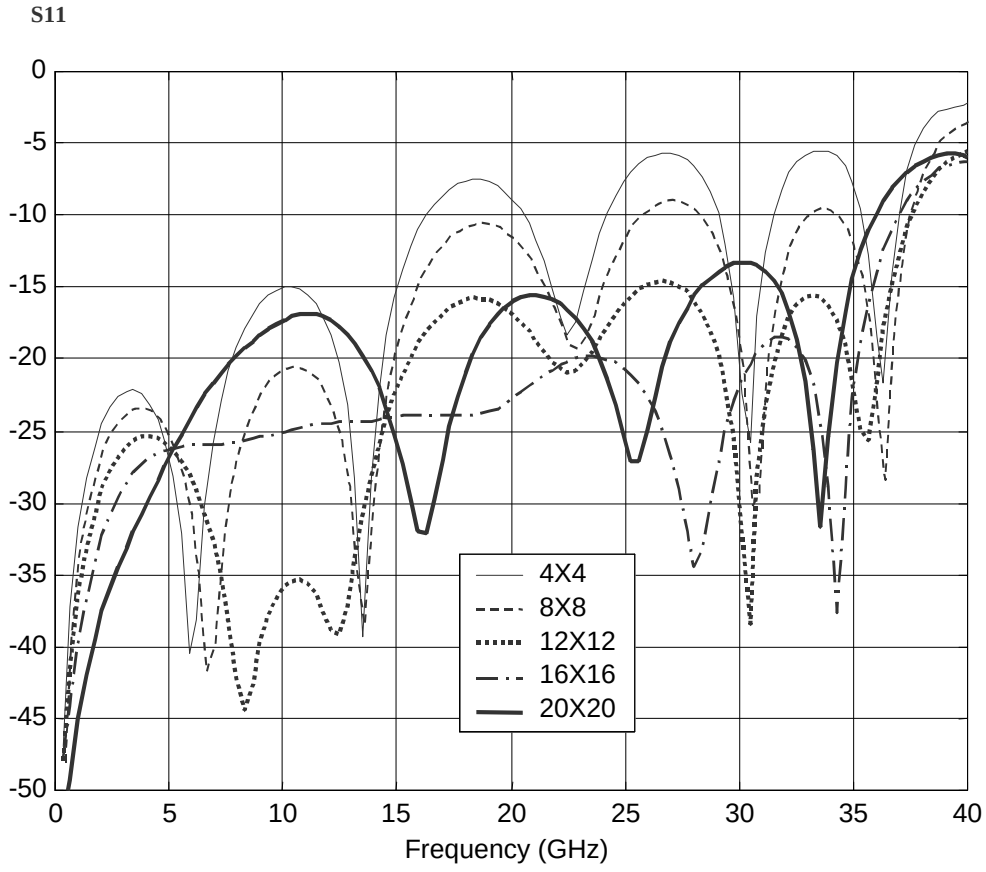

Figure 3. S11 for different ball cross section: 4x4, 8x8, 12x12, 16x16, 20x20 mil.